**Answers to question 1:**

1.a i) Bookwork

Student must explain they are self-biased current references and explain the need and role of the startup circuit based on equations. [4 points]

Equation for output current:



If we self bias and force IIN/IO = 1 with top current mirror, then ln(1) = 0

Require IIN/IO > 1

In Figure 1.1, IIN/IO = n=2

So, assuming matched devices



[4 points]

Must elaborate that the circuit in Fig. 1.1 has a better temperature coefficient that that of fig 1.2 and show equations for Temperature coefficient.

Fig 1.1 is a Improved TCF using VT Referenced Current Source/Sink

 [1 point]

Fig 1.2 is a Vbe Referenced Sink/Source with a temperature coefficient:

 [1 point]

[Total 6 points]

b) For Fig 1.1:





[3 points]

For Fig 1.2



Assume VBE=0.7



[3 points]

[Total 6 points]

c. ) Bandgap voltage reference circuit which has almost zero temperature coefficient, used mainly as stable voltage reference in ICs.

[4 points for figure]

For BG reference,











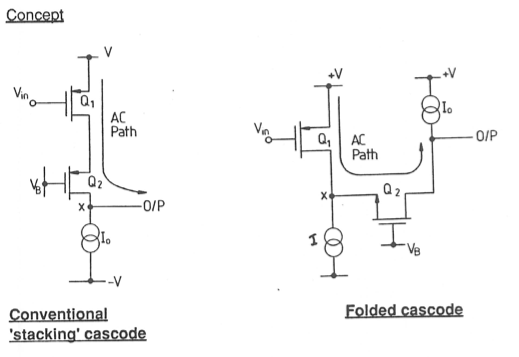


[4 points for derivation]

[Total 8 points]

**Answer to question 2:**

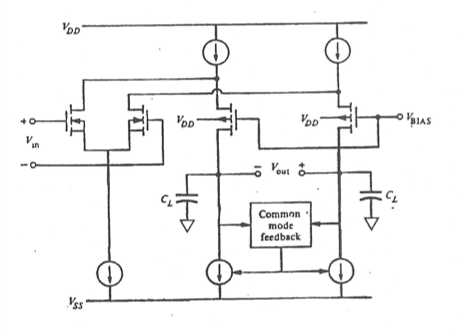
a)



In the folded cascode we are unstacking the conventional cascode and spreading it out. The AC current path is folded and this allow a reduction in power supply. The conventional cascode requires a 2-stage architecture and since the impedance at (x) is high requires internal compensation. The folded cascode can be used as a single stage architecture, node x is low impedance so the only high impedance node will be at the output.

Gain of the folded cascode Av=gm1/Go.

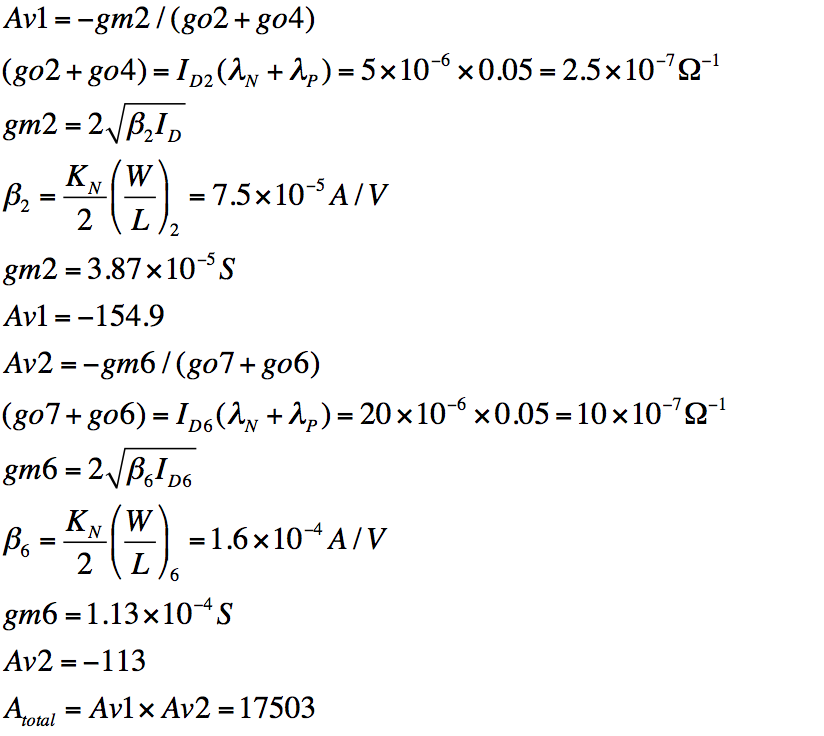
[2]



[4]

[Total 6 points]

b)



=1.76MHz

[8]

In a 2-stage opamp the load contributes to the 2nd pole hence reducing load increases stability.

With a single-stage, the load forms the dominant pole hence reducing the load increases bandwidth.

[2]

[Total 10 points]

c.

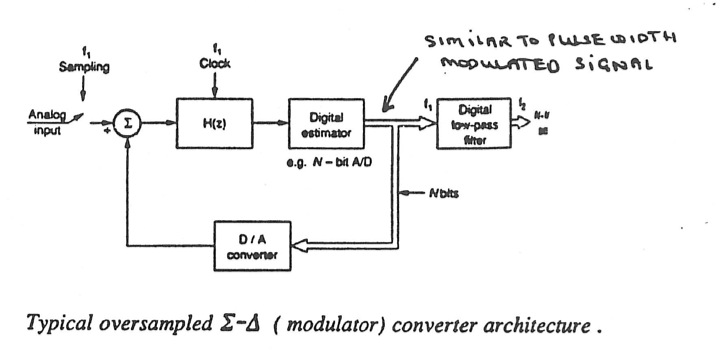




[Total 4 points]

**Answers to question 3:**

a) Explain sigma delta operation (bookwork).

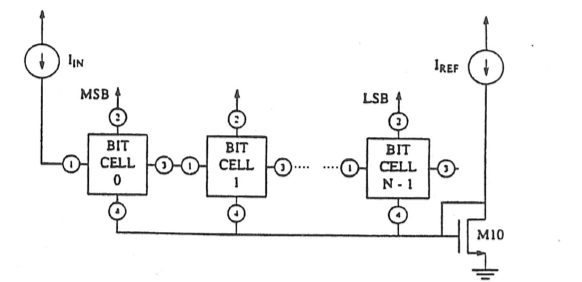
[5]

[5]

b)(i) Explain how the conversion works (bookwork)

[3]

Draw a cascade of blocks whereby N=8



[4]

c) KT/C noise limits the resolution of a sampled data converter.



[3]

**Answers to question 4:**

1. Operating conditions:

 [4]

The Bulk is not connected to the source due to void VBS from becoming a forward biased diode. [2]

[Total 6 points]



[3]





[3]

[Total 6 points]

[5]

[3]

[Total 8 points]

**Answer to question 5**

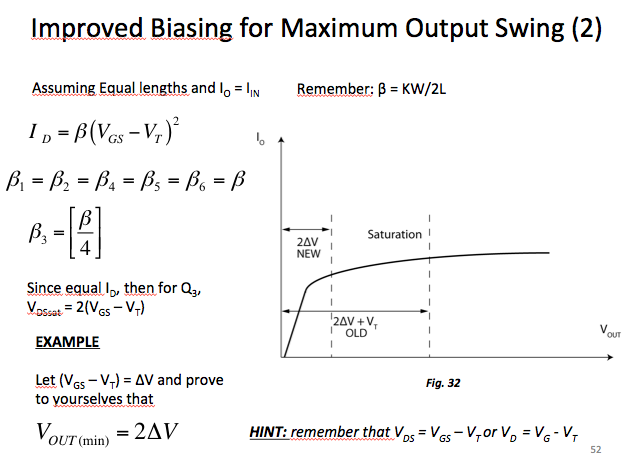
1. Regulated Cascode:

[4]

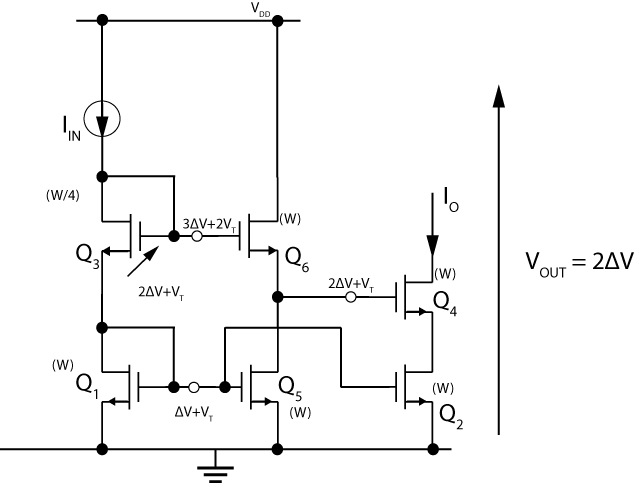
A regulated cascode current sink/source. The drain-source voltage of Q1 is regulated by the feedback amplifier Q2. It has a very high output impedance as a result equivalent to that of a double cascode. [2]

[Total 6 points]

b. From notes:



Annotation of VGS’ of each transistor:



[Total 6 points]

c)The two and four transistor potential dividers depicted in figure below.



For the two transistor potential divider





For the four transistor potential divider











The aspect ratio of the transistors in the four-transistor potential divider is much less than the two-transistor circuit, therefore, its consuming area will be less. For example, assuming common width of 10 units, for the two transistor configuration the active area becomes 10\*(64+136)=2000 units while for the four transistor it becomes 10\*2\*(10+19.125)=582.5 units.

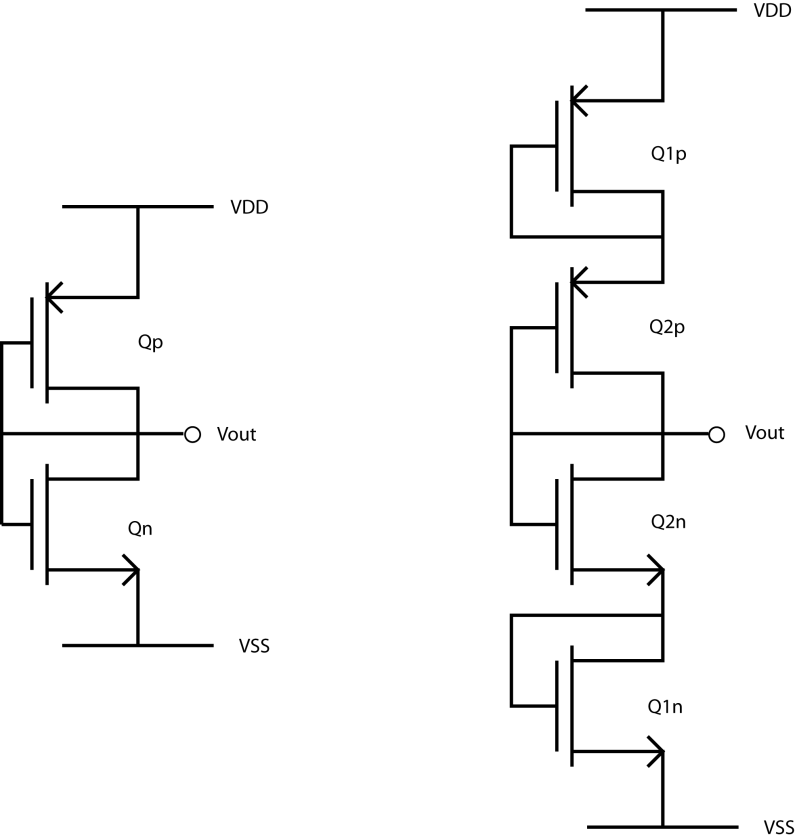


Figure 1. Answer to Question 2.b; potential Divider circuits

Drawing the potential divider with two transistor [2]

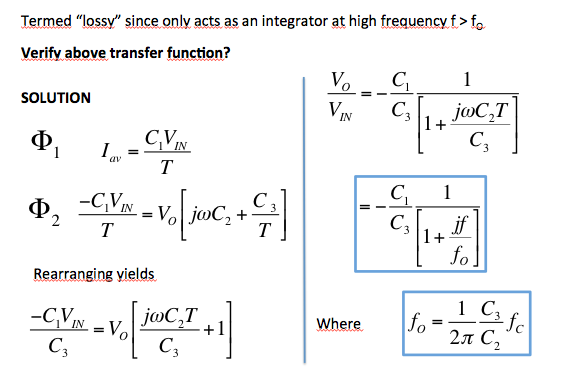
Drawing the potential divider with four transistor [2]

Calculating the required transistor sizes for each potential divider and comparing their area [4]

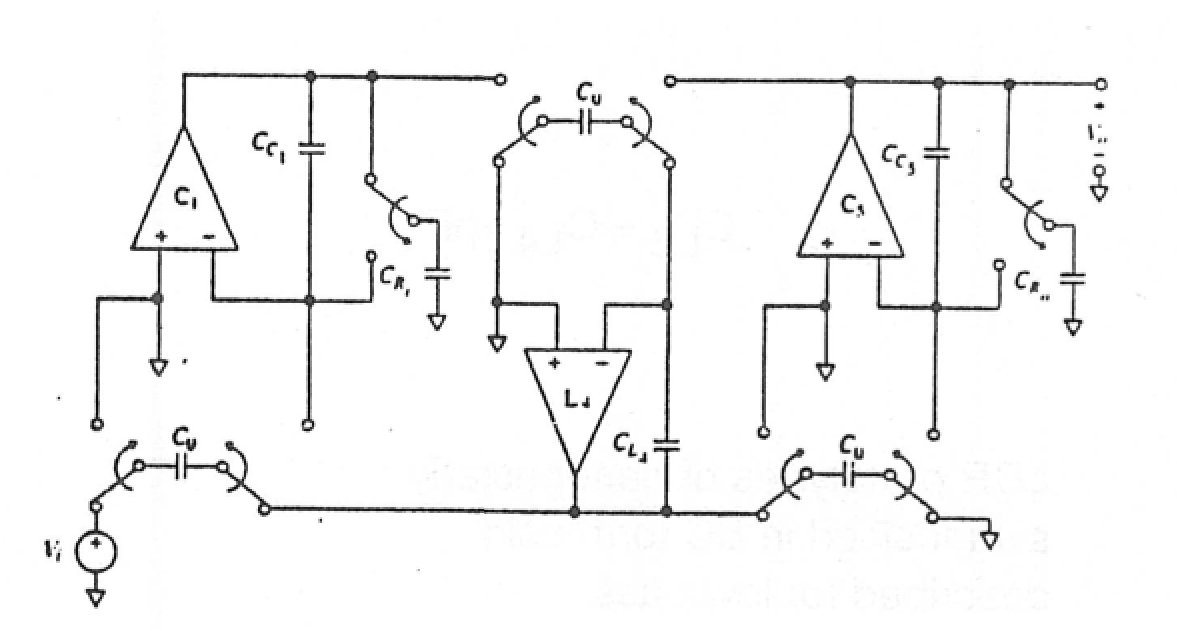
[Total 8 points]

**Answer to question 6**

a)Derivation from notes

[10]

b. (i) 3rd-order Chebyshev low pass switched-capacitor ladder filter.



[5]

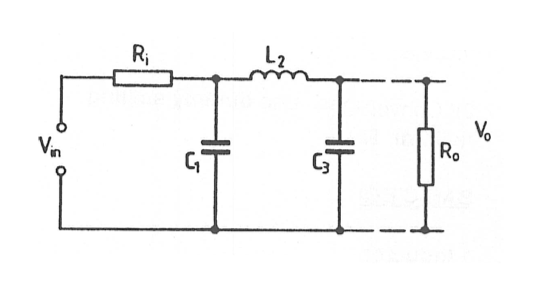
General transformation rules for ladder prototypes:

Inductor: 

Capacitor: 

Resistor Rs=dummy scalar.

The circuit is equivalent to an RLC prototype



[5]

ii. For switched capacitor equivalent:

Cc1=Cc3=5.08 pF

CL2=3.49 pF.

Cu=1pF

Assume scaling Rs=Ri=Ro=1Ω

Therefore

L2= CL2/fc= 3.49/100x103=3.49x10-5 H

Normalised 1rad/sec we multiply by 2πf0

L2=3.49 x10-5 x 2π x 5 KHz =1.096 H

C1=C3=Cc3/fc = 5.08/100x103 =5.08x10-5 f

Normalised value C1=C3=1.596